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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,461	10/30/2003	Martin A. Cotton	8245.061	7982

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EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/697,461	COTTON, MARTIN A.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,9-12,17-21,23-26,29 and 30* is/are pending in the application.

4a) Of the above claim(s) *17-20 and 29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *2,9-12,21,23-26 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 2, 9-12, 21, 23-26, and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by US 5,677,515 (Selk).

Selk discloses, referring primarily to figures 3a and 3b, a printed circuit board having an EMI shielding structure for shielding wiring circuit traces on a plurality of circuit trace layers applied on a plurality of printed circuit board layers and electrically isolated there between by the printed circuit board layers and having a printed circuit board multi-layer structure, characterized by: a trench (72, 74) having a rim about an opening of the trench at a top printed circuit board layer and said trench extending through a plurality of printed circuit board layers to a grounding plane (50) exposing said grounding plane and said trench having an interior wall with a conductive plating material (70) applied over said interior wall and said trench having a length greater than two times a breadth of said trench and wherein the trench completely surrounds an area (col. 4, lines 45-55) and extends adjacent to the perimeter of the printed circuit board

(see figure 3b) and wherein said conductive plating material electrically connects to said exposed grounding plane [claim 2].

Additionally, Selk discloses, a printed circuit board having a reference plane structure for fixing a potential reference for a plurality of wiring circuit trace layers that are electrically isolated there between by a plurality of printed circuit board layers and having a printed circuit board layer with a main surface, characterized by: a wire trace circuit layer (44) applied to said main surface; a printed circuit board insulation layer (62) formed over said wire trace circuit layer; a reference plane (50) applied over the printed circuit board insulation layer; a trench (72, 74) having an interior wall extending through and exposing the wire trace circuit layer, and the trench further extending through the insulation layer to the reference plane wherein the reference plane is exposed and wherein the trench completely surrounds an area and extends adjacent to the perimeter of the printed circuit board layer (col. 4, lines 50-55); and a conductive plating layer (70) on the interior wall electrically connects the wire trace circuit layer to the reference plane [claim 9], wherein the trench completely encompasses the wire trace circuit layer (col. 4, lines 50-55) [claim 10], wherein the reference plane is fixed at a ground potential (see col. 4, lines 55-65) [claim 11], wherein the reference plane is fixed at a reference voltage (see col. 4, lines 55-65) [claim 12].

Also, Selk discloses, referring primarily to figures 3a-4c, a printed circuit board having an EMI shielding structure for shielding a plurality of wire trace layers, characterized by: a printed circuit board layer having a wire trace (44) applied thereto; an insulation layer (66); and a grounding plane (50); a first trench (72, 74) having an

interior wall and forming a perimeter completely surrounding the wire trace (col. 4, lines 50-55), the first trench extending adjacent to the perimeter of the printed circuit board layer, extending through the printed circuit board layer and extending to the ground plane and exposing said ground plane; and an electrically conductive plating material (70) applied upon the interior wall of the first trench and electrically connecting to the exposed ground plane providing a perimeter shield for the trace [claim 21], further characterized by: a second trench (72', 74') having an interior wall and spaced a distance from the first trench such that the wire trace extends between the first trench and second trench, the second trench extending through the printed circuit board said ground plane, layer and extending to the ground plane exposing said ground plane wherein the interior wall of the second trench is plated with an electrically conductive plating material electrically connecting to the exposed ground plane thereby providing a double trench shield (figure 4b, col. 4, lines 60-65) [claim 23], further characterized by: an EMC sensitive track of conductive material (44) extending wholly within a perimeter defined by the first trench and disposed between a plurality of circuit board insulation layers through which the first trench extends [claim 24].

Moreover, Selk discloses, a printed circuit board having an EMI shielding structure for shielding a plurality of wire trace layers, characterized by: a plurality of printed circuit board layers having a plurality of wire trace layers, each printed circuit board layer separated by an insulation layer and having a grounding plane layer; and a first trench (72, 74) completely surrounding an area (col. 4, lines 50-55) and extending adjacent to the perimeter (figure 3b) and extending from a top printed circuit board layer

to the grounding plane layer (50), the first trench having an electrically conductive plating (70) applied over an interior wall of the first trench and electrically connecting to the ground plane [claim 25], further characterized by: a second trench (40B-1) disposed interior to the first trench and said second trench extending substantially in parallel to the first trench; and the second trench having an electrically conductive plating (52) applied over an interior wall thereof electrically connecting to the ground plane and an EMC sensitive track (33B) extending in a printed circuit board layer positioned between the first trench and the second trench [claim 26].

Furthermore, Selk discloses, a printed circuit board having an EMI shielding structure for shielding a plurality of wire trace layers, characterized by: a plurality of printed circuit board layers having a plurality of wire trace layers, each printed circuit board layer separated by an insulation layer and having a grounding plane layer (50); a first trench (72, 74) extending from a top printed circuit board layer to the grounding plane layer and the first trench having an electrically conductive plating (70) applied over an interior wall of the first trench and electrically connecting to the ground plane and wherein the first trench completely surrounds an area of the printed circuit board (col. 4, lines 50-55); and a second trench disposed interior to the first trench and said second trench extending substantially in parallel to the first trench (figure 4a) and the second trench having an electrically conductive plating applied over an interior wall thereof electrically connecting to the ground plane; and at least two EMC sensitive tracks (42, 44) extending in a printed circuit board layer positioned between the first trench and the second trench [claim 30].

Response to Arguments

Applicant's arguments filed 4 May 2007 have been fully considered but they are not persuasive. Applicant alleges "However, as shown in Attachment 1 submitted herewith, first and second grooves 72' and 74' of Fig. 3b do not completely surround the signal layer 42. As indicated presently in Attachment 1, the first and second grooves 72' and 74' extend completely to the edge of the wiring board 40. Gaps at the right hand edge of the board, represented by added reference letters A and B, indicate portions of the wiring board 40 which are not surrounded by the grooves, thus the signal layer 42 is not completely surrounded by the first and second grooves 72' and 74'; contrary to the present claims. Selk thus does not teach each and every element of the claimed invention as required under 35 U.S.C. §102". However, the ordinarily skilled artisan would understand that figure 3b is a partial perspective view of the device of Selk and thus the portions indicated by 'A' and 'B' in Applicant annotated version of Selk figure 3 is not the edge of the device but rather a mid portion of the device. Moreover, regarding the groves 72 and 74, Selk expressly states (col. 4, lines 51-53):

> "These grooves may be further joined beyond the termination points of the of the signal traces and thereby further surround the signal layer."

Thus it would be readily apparent to the ordinarily skilled artisan that the grooves 72 and 74 cooperate to completely surround the signal layer and thus meet the claimed limitation that an area of the circuit board be completely surrounded. Hence, Applicant's traversal of the instant rejection on this ground is deemed unsuccessful.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeremy C. Norris
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JCSN